

AMENDMENTS TO THE CLAIMS:

1-2. (Canceled)

3. (Currently amended) The method according to claim 40, wherein the netlist modification is divided into a set of steps, each step addressing a specific ~~aspect~~ domain of the design space.

4-5. (Canceled)

6. (Currently amended) The method according to claim 40, wherein the modification affects multiple objectives and constraints which involve physical placement, electrical properties, and logical ~~data~~ circuitry.

7-11. (Canceled)

12. (Previously presented) The method according to claim 40, further comprising: at predetermined stages of the method, selectively determining whether to intercept the method and implement the most recently considered netlist modification and cell placement.

13-23. (Canceled)

24. (Currently amended) The system according to claim 46, wherein the netlist

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modification is divided into a set of steps, each step addressing a specific ~~aspect~~domain of the design space.

25-26. (Canceled)

27. (Currently amended) The system according to claim 46, wherein the modification affects physical placement, electrical properties, and logical ~~data~~circuitry.

28-32. (Canceled)

33. (Previously presented) The system according to claim 46, further comprising:
a unit for selectively determining, at predetermined stages of the process, whether to intercept the process and implement the most recently considered netlist modification and cell placement.

34-39. (Canceled)

40. (Currently amended) A method of modifying a plurality of domains of a circuit in a design space, the domains including at least one of a Boolean domain, an electrical domain, and a physical domain, and the circuit comprising a plurality of cells, said method comprising:

(a) considering a possible netlist modification for the design space;

(b) considering a cell placement for the modified netlist;

(c) before implementing the considered netlist modification and the considered cell placement, determining whether the considered netlist modification and the considered cell placement improve at least one domain of the design space, while leaving all other domains of the design space satisfactory; and

(d) if the considered netlist modification and the considered cell placement improve at least one domain of the design space, while leaving all other domains of the design space satisfactory, implementing the considered netlist modification and the considered cell placement, but if the considered netlist modification and the considered cell placement do not improve at least one domain of the design space, while leaving all other domains of the design space satisfactory, returning to (a).

41. (Previously presented) The method according to claim 40, wherein considering a cell placement comprises considering a plurality of placement techniques.

42. (Previously presented) The method according to claim 40, wherein the design space is divided into bins, and (a) through (c) are performed on a bin.

43. (Previously presented) The method according to claim 40, wherein (c) further comprises determining whether further improvement of the design space should be sought; and, if so, returning to (a).

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44. (Previously presented) The method according to claim 40, further comprising making an initial layout for the design space.

45. (Previously presented) The method according to claim 40, further comprising storing information to update data about the implemented netlist and cell placement.

46. (Currently amended) A system for modifying a plurality of domains of a circuit in a design space, the domains including at least one of a Boolean domain, an electrical domain, and a physical domain, and the circuit comprising a plurality of cells, said system comprising:

~~(a)~~-a unit for considering a possible netlist modification for the design space;

~~(b)~~- a unit for considering a cell placement for the modified netlist;~~and~~

~~(c)~~-a unit for determining whether the considered netlist modification and the considered cell placement improve at least one domain of the design space, while leaving all other domains of the design space satisfactory; and

a unit responsive to a determination that the considered netlist modification and the considered cell placement improve at least one domain of the design space, while leaving all other domains of the design space satisfactory, for implementing the considered netlist modification and the considered cell placement, said unit further responsive to a determination that the considered netlist modification and the considered cell placement do not improve at least one domain of the design space, while leaving all other domains of the design space satisfactory, for inhibiting implementing of the considered netlist modification and the considered cell placement.

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47. (Canceled)
48. (Previously presented) The system according to claim 46, further comprising a unit for making an initial layout for the design space.
49. (Previously presented) The system according to claim 46, further comprising a unit for storing data about the implemented netlist and cell placement.
50. (Currently amended) A programmable storage medium tangibly embodying a program of machine-readable instructions for a method executable by a digital processing apparatus to modify a plurality of domains of a circuit in a design space, the domains including at least one of a Boolean domain, an electrical domain, and a physical domain, and the circuit comprising a plurality of cells, said method comprising:
- (a) considering a possible netlist modification for the design space;
 - (b) considering a cell placement for the modified netlist;
 - (c) before implementing the considered netlist modification and the considered cell placement, determining whether the considered netlist modification and the considered cell placement improve at least one domain of the design space, while leaving all other domains of the design space satisfactory; and
 - (d) if the considered netlist modification and the considered cell placement improve at least one domain of the design space, while leaving all other domains of the design space

satisfactory, implementing the considered netlist modification and the considered cell placement, but if the considered netlist modification and the considered cell placement do not improve at least on domain of the design space, while leaving all other domains of the design space satisfactory, returning to (a).

51. (Previously presented) The programmable storage medium according to claim 50, wherein considering a cell placement comprises considering a plurality of placement techniques.

52. (Previously presented) The programmable storage medium according to claim 50, wherein the design space is divided into bins, and (a) through (c) are performed on a bin.

53. (Previously presented) The programmable storage medium according to claim 50, wherein (c) further comprises determining whether further improvement of the design space should be sought; and, if so, returning to (a).

54. (Previously presented) The programmable storage medium according to claim 50, wherein the method further comprises making an initial layout for the design space.

55. (Previously presented) The programmable storage medium according to claim 50, wherein the method further comprises storing information to update data about the implemented netlist and cell placement.

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56. (New) The programmable storage medium according to claim 50, wherein the netlist modification is divided into a set of steps, each step addressing a specific domain of the design space.

57. (New) The programmable storage medium according to claim 50, wherein the modification affects multiple objectives and constraints which involve physical placement, electrical properties, and logical circuitry.

58. (New) The programmable storage medium according to claim 50, wherein at predetermined stages of the method, the method selectively determines whether to intercept the method and implement the most recently considered netlist modification and cell placement.